REMARKS

In response to paragraph 2 of the Office Action supplemental Declarations are herein enclosed.

In response to paragraph 4 of the Office Action: In accordance with 1.173(a)(2) a clean copy of the drawings were submitted with the reissue application. The Applicants believe that the submitted drawings are in accordance with 1.84 and no further drawings will be required.

Claim 1 was objected to because of a capitalization informality. Claim 1 has been amended ábove. In addition, claims 1,2,5,9,26,27, and 35, have been amended above to their original patent form. Claims 1,2,5,9,26,27, and 35 have been returned to their original patented, pre-reissue form (with the exception of a capitalization correction in Claim 1) in order to avoid issues of intervening rights. New claims 40-58 have been added above. New claims 40-43,52,53, and 58, generally correspond to Claims 1,2,5,9,26,27, and 35 as amended in the reissue application filed 9/21/00. Claims 36-39 have been deleted above without prejudice. Claims 1-35, and 40-58, are now pending in this case.

Support for added independent claims 40,52,53, and 58 may be found in the specification as claims 1,26,27, and 35, respectively; and also in Figures 3A, 3B, 3C, 4, 10, 11, and 12. Support for added dependent claims may be found in the specification as claims 2,5,6,8,9,12,13,19,20,21,24,28,29,31, and 34.

Claims 1-39 were rejected under 35 U.S.C. sec. 251 as being based upon a defective reissue declaration, and as being an improper recapture. Claims 1-35 were rejected under 35 U.S.C. sec. 112, first paragraph. Claims 1,5,22, and 36 were rejected under 35 U.S.C. 102(b) as being anticipated by Hegel, Jr. et al. (U.S. 004752694A). Claims 6, 7, 12, 13, 15, 19, 24, and 25 were rejected under 35 U.S.C. 103(a) as being unpatenable over Hegel, Jr. et al.

35 U.S.C. § 251 Rejections

The rejection under 35 U.S.C. § 251 as being based upon a defective reissue declaration is overcome by the newly submitted re-executed inventors' declaration.

The Examiner has rejected claims 1-39 as being an improper recapture of broadened claimed subject matter surrendered during prosecution of the original application for the patent upon which the present reissue is based. Specifically, the Examiner points to amended reissue claims 1,2,5,9,26, and 35(now claims 40,41,42,43,52, and 58, respectively) as deleting the limitation "parallel connected" which then renders the reissue claims as broader in scope than the issued patent claims. The Examiner points to the language used by the first Examiner in allowing the original application ("...the means for correcting specified by independent claim 2,24,33, or 37.") and MPEP sec. 1412.02, and states that the applicants previously surrendered the now broader aspect of the reissue

claims during prosecution of the original application since the Applicants did not present on the record a counter statement or comment as to the Examiner's reasons for allowance.

Indeed, the reference MPEP section does indicate, by way of example, that an applicant has surrendered a limitation if that limitation is part of an Examiner's reason for allowance (MPEP sec. 1412.02, Example C). But, the Applicants respectfully direct the Examiner's attention to the language in Example A of the same MPEP section. Here the example is directed towards an applicant arguing the limitation. However, the MPEP points out that the argument must be specific to the limitation and not a general statement. MPEP page 1400-0, col. 1, lines 7-17, states:

> "The argument that the claim limitation defined over the rejection must have been specific as to the limitation; rather than a general statement regarding the claims as a whole. In other words, a general 'boiler plate' sentence will not be sufficient to establish recapture."

Keeping this MPEP rule in mind, it appears that the present Examiner has mischaracterized the first Examiner's reasons for allowance. The first Examiner states that the prior art did not teach or suggest a system "having in combination with other required elements, the means for correcting". It is clear that (1) this was a general statement by the first Examiner and (2) that the first Examiner did not specifically state the limitation of "parallel connected" in the reason for allowance. Indeed, nowhere in the Notice of Allowability does

the word "parallel" appear. The first Examiner's reason for allowance was the "combination" of a means for correcting with the other elements of the claim; not to the specific "parallel connection" recited in the means for correcting. The first Examiner's statement can only be regarded as a general statement regarding a combination of the means for correcting with other elements of the claim, not a specific statement regarding "parallel connection".

This specific statement requirement is clearly illustrated in the MPEP sec. 1412.02, example C, which requires "limitation A" to be stated in the Examiner's reason for allowance in order to prevent "limitation A" from being omitted in the reissue claim. In the present case the limitation being omitted (i.e., "limitation A") is "parallel connected". Yet, the first Examiner's reason for allowance did not state that the reason for allowance was because of the limitation "parallel connected" as in Claim 1 (now claim 40). The first Examiner's reason for allowance was because of a "combination with other required elements" of the means for correcting. The first Examiner's reason for allowance is not specific to the limitation: "parallel connected".

Therefore, the Applicants respectfully submit that the now broader reissue claims without the limitation "parallel connected" is not impermissible recapture of surrendered subject matter and that Claims 40-43, 52 and 58, are patentable and should be allowed.

The present Examiner also states the reissue Claim 27 (now claim 53) deletes a limitation, i.e., "capacitors" thus

rendering the reissue claim broader than the patent claim. The Examiner also states that the Applicant surrendered this broader aspect during the prosecution of the original application.

The Applicants respectfully point out that the word "capacitors" does not appear in the first Examiner's reason for allowance and that the first Examiner's reason for allowance was a general statement; that this general statement is not specific as contemplated by the MPEP sec. 1412.02. Therefore, the Applicants respectfully submit that the broadened aspect of the present reissue Claim 53 is not previously surrendered subject matter and that the present reissue Claim 53 is patentable and should be allowed.

35 U.S.C. sec. 112, first paragraph

Claims 1-35 were rejected as containing subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors had possession of the claimed invention.

The Examiner states that the specification does not describe a system in which the circuit elements are not parallel connected. Specifically, the Examiner points to figures 3B and 3C where there is shown a plurality of circuit elements, i.e., capacitors and switches, parallel connected, and indicates that the specification does not support any other interpretation other than a parallel connection.

First, it should be recognized that capacitors C_0, C_1, $C_2...C_N$, and their associated switches S_0, S_1, $S_2...S_N$, represent the offset correction circuit 220 shown in figure 3B, which is only a preferred implementation and not a limitation to only plural, parallel connected capacitors and switches. This is made clear by recognizing that the series representations (i.e., C_0, C_1, $C_2...C_N$, and S_0, S_1, $S_2...S_N$) are well known in the art and that the identifying variable N can range from integer value 0 to any positive integer value. Moreover, it is clear that for N = 0, there is only one capacitor and switch branch, which by definition, cannot be "parallel connected". Likewise, if N > 0 but only one switch in figure 3B, S_0 for example, is closed, and all the other switches S_1-S_N are open, then only one branch is connected. Which again means that the branch cannot be in parallel with the other branches. In this situation (only S_0 closed) there is only one functioning capacitor, C_0; capacitors C1-CN are not functionally operational; and the system is only using the capacitance associated with capacitor C_0.

The Examiner also states, with regard to current sources, that the specification does not describe a system in which the circuit elements are not parallel connected. The Applicants respectfully point out that the current sources are similarly represented as $I_0...I_N$ and that even one moderately skilled in the art recognizes that N can be any value 0 to any positive integer; and that for a N=0 situation there is only one current branch which by definition cannot be parallel connected. Thus, again, to one even moderately skilled in the

art, the specification more than reasonably conveys the Applicants had possession of the claimed invention.

35 U.S.C sec. 102(b) Rejections

Claim 1 of the present application recites an infrared imaging system. The claimed system comprises an infrared focal plane array, which in turn comprises a plurality of infrared detector elements arranged in an array. In addition, Claim 1 also recites means for separately correcting offsets in the detection signals to compensate for nonuniformities in the detector elements. Nowhere does Hegel disclose or suggest applying offsets to the detection signals. Indeed, Hegel's figure 1 shows the output of the detectors 11 through diodes D and then through a FET to point B. Nowhere in this path is an offset applied. Moreover it is clear from Hegel's description that since the FETs (44-46) are biased either full-on or full-off, there is effectively an electrical short between the diodes and point B (col. 2, lines 22-53) and no suggestion of any offset corrections.

The Examiner states that Hegel's memory (fig. 1, item 70) stores offset correction values. The Applicants respectfully disagree and point out that what Hegel's memory holds is biasing values for controlling how much current is allowed to flow through a particular Hegel detector. Clearly, controlling current flow through a device and applying offsets to the output of a device are not the same. Nor, as pointed out, does

Hegel, disclose or suggest applying offsets. Therefore, Claim 1 is patentable and should be allowed.

Claim 5 of the present application recites the feature of the having a number of switches equal in number to the number of circuit elements. The Examiner rejected Claim 5 by pointing to Hegel's switches A, B, and C. As pointed out above, and repeated here, these Hegel switches control current flow through the detectors and do not apply offsets as recited in the present Claim 5. Nowhere does Hegel disclose or suggest the application of offsets. Therefore Claim 5 is patentable and should be allowed.

Claim 21 of the present application recites timing means for providing focal plane timing signals to the readout circuit. The Examiner states that Hegel anticipates this claim by providing "clock input" to the readout circuit. However, the only thing that Hegel says in this regard is that the sequencer provides the signals necessary to synchronize the operation of memory, switch, and the readout circuit. It will be appreciated that this is not the same as providing a timing signal to a readout circuit to control readout and offset correction. Particularly, when Hegel does not disclose or suggest anything about offset corrections. Therefore, Claim 21 is patentable and should be allowed.

Claim 22 of the present application recites the features that the readout circuit comprises offset correction logic means for controlling the means for correcting in response to the timing signals presented to the readout circuit. As pointed out above, and repeated here, Hegel does not provide timing signals to the readout circuit or suggest offset correction

logic means for controlling the means for correcting. Therefore, Claim 22 is patentable and should be allowed.

35 U.S.C. sec. 103(a) Rejections

Claim 6 of the present application recites the features of storing offset correction values in binary form. Since Hegel does not disclose or suggest anything about offset correction values, binary or otherwise, Claim 6 is patentable and should be allowed.

Claim 7 of the present application recites the feature of storing a separate binary offset for each detector. As pointed out earlier, Hegel does not disclose or suggest applying offsets and consequently does not disclose or suggest anything about storing binary offsets; therefore Claim 7 is patentable and should be allowed.

Claim 12 of the present application recites the features of forming the detector array and the readout circuit on a single monolithic integrated circuit chip. The Examiner rejected this claim with the statement that it would have been obvious to one of ordinary skill to form on a single monolithic IC the system illustrated by Hegel. With regards to Hegel's system that may be true, however, whether or not Hegel's system could be formed on a monolithic IC has no bearing on whether or not the present invention could be formed on a monolithic IC. Therefore, Claim 12 is patentable and should be allowed.

Claim 13 of the present application recites the feature that the detector elements of Claim 1 comprise micro-bolometer detector elements. In rejecting this Claim the Examiner points to Hegel and states that Hegel is a bolometer and that the choice of size is a choice within the ordinary skill in the art. However, Hegel does not disclose or suggest applying offsets to the Hegel bolometers and, by extension, Hegel does not disclose applying offsets to micro-bolometers. Therefore, Claim 13 is patentable and should be allowed.

Claim 15 of the present application recites the feature of a fixed voltage source coupled to the micro-bolometers recited in Claim 13. As noted, the micro-bolometers of the present application are well beyond the ordinary skill represented in Hegel and that Hegel does not disclose or suggest applying offsets to such micro-bolometers. Therefore, Claim 15 is patentable and should be allowed.

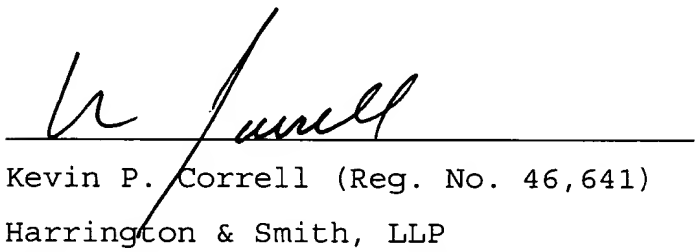
Claim 19 of the present application recites the feature of the output means comprising one or more buffers. In rejecting this claim, the Examiner states that it would have been obvious to one of ordinary skill to include buffers in view of the circuit protection that would have been provided. However, the Applicants point out that buffers are not just for circuit protection and the inclusion of such is not obvious. Moreover, the Applicants assert that the first prong of establishing a prima facie case of obviousness has not been met. First, there is no suggestion in Hegel to add such buffers nor is it obvious to one skilled in the art to simply add buffers to Hegel. Indeed, adding buffers could cause synchronization problems, increase current drain, increase operating

temperature, and so on. Clearly, adding buffers is not an obvious or trivial step. Therefore, since it would not be obvious to add buffers to Hegel, and Hegel does not disclose or suggest adding buffers, Claim 19 is patentable and should be allowed.

Enclosed is a check for $606.00 for four independent claims in excess of three and 15 claims in excess of twenty. Please charge deposit account 501924 for any fee deficiency.

For all of the foregoing reason, it is respectfully submitted that all of the claims now present in the application are clearly novel and patentable over the prior art of record. Accordingly, favorable reconsideration and allowance is respectfully requested. Should any unresolved issue remain, the Examiner is invited to call Applicants' Attorney at the telephone number indicated below.

Respectfully submitted,



10/24/01

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